# High- κ Dielectric & Metal Gate

## Moore's Law

- Moore's law is the observation that over the history of computing hardware, the number of transistors on integrated circuits doubles approximately every two years.

## Transistor Scaling

- It is the process of reducing transistor physical gate length.

## Challenges in Transistor Scaling

- $SiO_2$ has been used as a gate oxide material for decades. As transistors have decreased in size, the thickness of the $SiO_2$ gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current, raising device performance. As the thickness scales below 2nm, leakage currents due to tunneling increase drastically, leading to high power consumption, power loss and reduced device reliability. Replacing the $SiO_2$ gate dielectric with a high-κ material allows increased gate capacitance without the associated leakage effects.

## High- κ Materials

- **κ** is a dielectric constant, a measure of how much charge a material can hold.
- High-κ dielectric refers to a material with a high dielectric constant κ (as compared to $SiO_2$).

## Drain Current

- ***W*** *is the width of the transistor channel.*
- ***L*** *is the channel length.*
- ***M*** *is the channel carrier mobility.*
- $C_{inv}$ *is the capacitance density associated with the gate dielectric.*
- $V_G$ *is the voltage applied to the transistor gate.*
- $V_{th}$ *is the threshold voltage.*

$$I_{D,Sat} = \frac{W}{L}\mu C_{inv}\frac{(V_G - V_{th})^2}{2}$$

The term $V_G - V_{th}$ is limited in range due to reliability and room temperature operation constraints, since a too large $V_G$ would create an undesirable, high electric field across the oxide. Furthermore, $V_{th}$ cannot easily be reduced below about 200 mV, because leakage currents due to increased oxide leakage, and subthreshold conduction raise stand-by power consumption to unacceptable levels. Thus, according to this simplified list of factors, an increased $I_{D,sat}$ requires a reduction in the channel length or an increase in the gate dielectric **capacitance**.

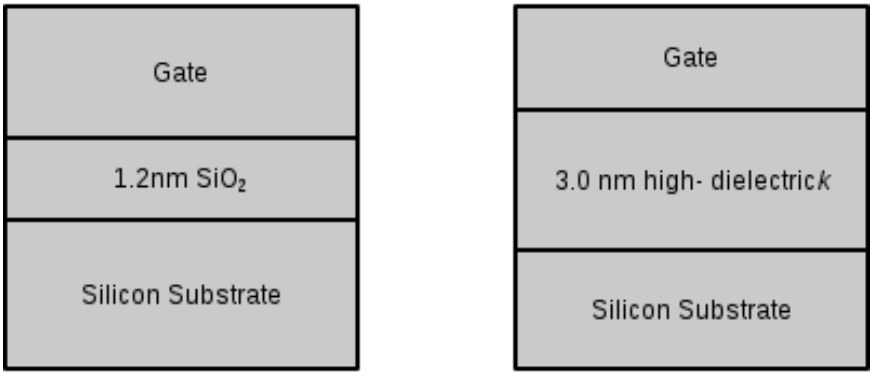
## Capacitance

$$C = \frac{\kappa \varepsilon_0 A}{t}$$

- ***A*** *is the capacitor area*
- ***κ*** *is the relative dielectric constant of the material (3.9 for silicon dioxide)*
- ***$\varepsilon_0$*** *is the permittivity of free space*
- ***t*** *is the thickness of the capacitor oxide insulator*

Since leakage limitation constrains further reduction of *t*, an alternative method to increase gate capacitance is altering κ by replacing silicon dioxide with a high-κ material. In such a scenario, a thicker gate oxide layer might be used which can reduce the leakage current flowing through the structure as well as improving the gate dielectric reliability.

## Result of using High- κ Materials




Existing 90nm Process
Capacitance = 1x
Leakage Current = 1x

A potential high- process*k*
Capacitance = 1.6x
Leakage Current = 0.01x

| | | |
|---|---|---|
| **Capacitance** | 60% Increase | • Faster Transistors |
| **Leakage Current** | 99% Reduction | • Less Power Consumption<br>• Less Power loss<br>• Less Heat Generation |

## Challenges of using High- κ Materials with Poly-Si

- High threshold voltage because of Fermi level pinning at poly-Si/High-K interface.
- Degraded channel carrier mobility due to Surface phonon scattering.
- High gate Resistance, Increasing the Delay (td=RC).
- Poly-Si gate depletion layer.

## Metal Gates

Metal gates instead of Poly-Si could solve the following problems

- Less defects at the surface solving the Fermi level pinning.
- Decrease surface phonon scattering.
- Less resistance compared to poly-Si.
- Decreasing depletion layer, leading to higher performance.

## Challenges of using Metal Gates

- Metal–gate electrodes with the correct work functions are required for high-performance.

## Breakthroughs with Metal Gates

- N-Type and P-Type metal with the CORRECT work functions on High-k have been engineered.
- High-K\Metal-Gate stack achieves N-MOS and P-MOS channel mobility close to $SiO_2$.
- High-K\Metal-Gate stack shows significantly lower gate leakage than SiO2.